# 74AHC2G125; 74AHCT2G125

## Dual buffer/line driver; 3-state

Rev. 3 — 6 May 2013 Product data sheet

## 1. General description

The 74AHC2G125 and 74AHCT2G125 are high-speed Si-gate CMOS devices. They provide a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (nOE). A HIGH at nOE causes the output to assume a high-impedance OFF-state.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

## 2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
  - HBM JESD22-A114E: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Specified from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74AHC2G125DP | –40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74AHCT2G125DP | | | | |
| 74AHC2G125DC | –40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74AHCT2G125DC | | | | |
| 74AHC2G125GD | –40 °C to +125 °C | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm | SOT996-2 |
| 74AHCT2G125GD | | | | |

## 4. Marking

**Table 2. Marking codes**

| Type number | Marking |
|---|---|
| 74AHC2G125DP | A25 |
| 74AHCT2G125DP | C25 |
| 74AHC2G125DC | A25 |
| 74AHCT2G125DC | C25 |
| 74AHC2G125GD | A25 |
| 74AHCT2G125GD | C25 |

## 5. Functional diagram

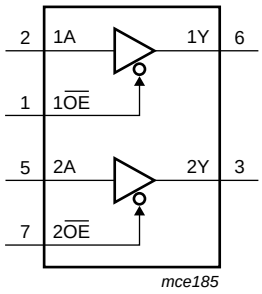



**Fig 1. Logic symbol**

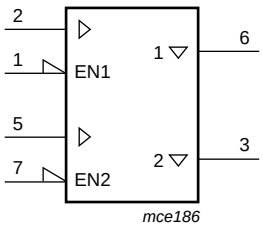



**Fig 2. IEC logic symbol**

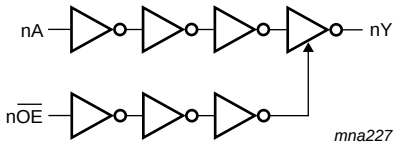



**Fig 3. Logic diagram (one buffer)**

## 6. Pinning information

### 6.1 Pinning

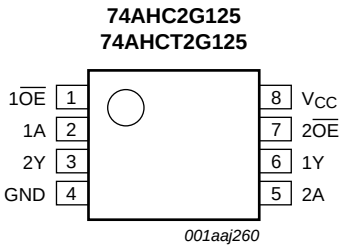
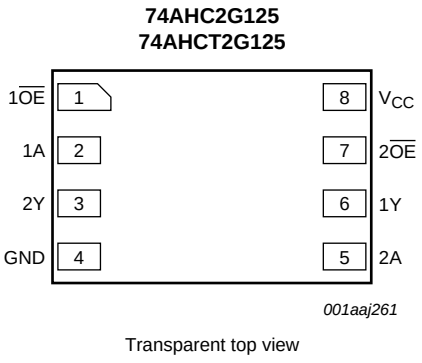



**Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)**




Transparent top view

**Fig 5. Pin configuration SOT996-2 (XSON8)**

### 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $1\overline{OE}$, $2\overline{OE}$ | 1, 7 | output enable input (active LOW) |
| 1A, 2A | 2, 5 | data input |
| GND | 4 | ground (0 V) |
| 1Y, 2Y | 6, 3 | data output |
| $V_{CC}$ | 8 | supply voltage |

## 7. Functional description

**Table 4. Function table[1]**

| Control | Input | Output |
|---|---|---|
| $n\overline{OE}$ | nA | nY |
| L | L | L |
| L | H | H |
| H | X | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7.0 | V |
| $V_I$ | input voltage | | | −0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V | [1] | −20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_O$ | output current | $-0.5$ V $< V_O < V_{CC} + 0.5$ V | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 75 | mA |
| $I_{GND}$ | ground current | | | −75 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [2] | - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of $P_{tot}$ derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of $P_{tot}$ derates linearly with 8 mW/K.
For XSON8 package: above 45 °C the value of $P_{tot}$ derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 74AHC2G125 | | | 74AHCT2G125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | - | - | 20 | - | - | 20 | ns/V |

## 10. Static characteristics

**Table 7. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC2G125** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –50 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = –8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8.0 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 0.25 | - | 2.5 | - | 10 | μA |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 10 | - | 40 | μA |

**Table 7. Static characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $C_I$ | input capacitance | | - | 1.5 | 10 | - | 10 | - | 10 | pF |
| **74AHCT2G125** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = –50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –8.0 mA | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 0.25 | - | 2.5 | - | 10 | μA |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 10 | - | 40 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = 3.4 V; other inputs at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| $C_I$ | input capacitance | | - | 1.5 | 10 | - | 10 | - | 10 | pF |

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*GND = 0 V; for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC2G125** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA to nY; see Figure 6 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.7 | 8.0 | 1.0 | 9.5 | 1.0 | 11.5 | ns |
| | | $C_L$ = 50 pF | | - | 6.6 | 11.5 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.4 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | $C_L$ = 50 pF | | - | 4.8 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |

**Table 8. Dynamic characteristics** *...continued*

*GND = 0 V; for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{en}$ | enable time | $n\overline{OE}$ to nY; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.0 | 8.0 | 1.0 | 9.5 | 1.0 | 11.5 | ns |
| | | $C_L$ = 50 pF | | - | 6.9 | 11.5 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.6 | 5.1 | 1.0 | 6.0 | 1.0 | 6.5 | ns |
| | | $C_L$ = 50 pF | | - | 4.9 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nY; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 6.0 | 9.7 | 1.0 | 11.5 | 1.0 | 12.5 | ns |
| | | $C_L$ = 50 pF | | - | 8.3 | 13.2 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.1 | 6.8 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| | | $C_L$ = 50 pF | | - | 5.7 | 8.8 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| $C_{PD}$ | power dissipation capacitance | per buffer; $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 9 | - | - | - | - | - | pF |
| **74AHCT2G125** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA to nY; see Figure 6 | [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.4 | 5.5 | 1.0 | 6.5 | 1.0 | 6.5 | ns |
| | | $C_L$ = 50 pF | | - | 4.8 | 7.5 | 1.0 | 8.5 | 1.0 | 8.5 | ns |
| $t_{en}$ | enable time | $n\overline{OE}$ to nY; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.9 | 5.1 | 1.0 | 6.0 | 1.0 | 6.0 | ns |
| | | $C_L$ = 50 pF | | - | 5.1 | 7.5 | 1.0 | 8.5 | 1.0 | 8.5 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nY; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.5 | 6.8 | 1.0 | 8.0 | 1.0 | 8.0 | ns |
| | | $C_L$ = 50 pF | | - | 6.1 | 8.8 | 1.0 | 10.0 | 1.0 | 10.0 | ns |

**Table 8. Dynamic characteristics** *...continued*

*GND = 0 V; for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $C_{PD}$ | power dissipation capacitance | per buffer; $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 11 | - | - | - | - | - | pF |

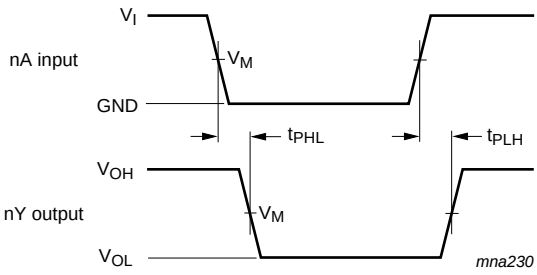
[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[2] Typical values are measured at $V_{CC}$ = 3.3 V.

[3] Typical values are measured at $V_{CC}$ = 5.0 V.

[4] $C_{PD}$ is used to determine the dynamic power dissipation $P_D$ (μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in Volts.

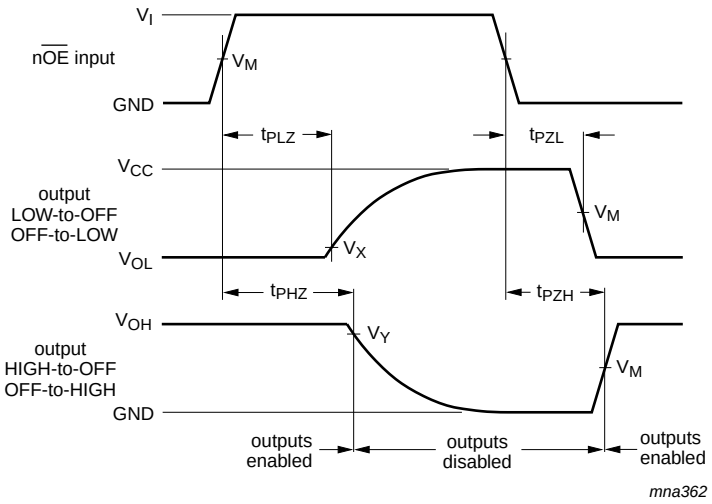
## 12. Waveforms




Measurement points are given in Table 9.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 6. Input (nA) to output (nY) propagation delays**



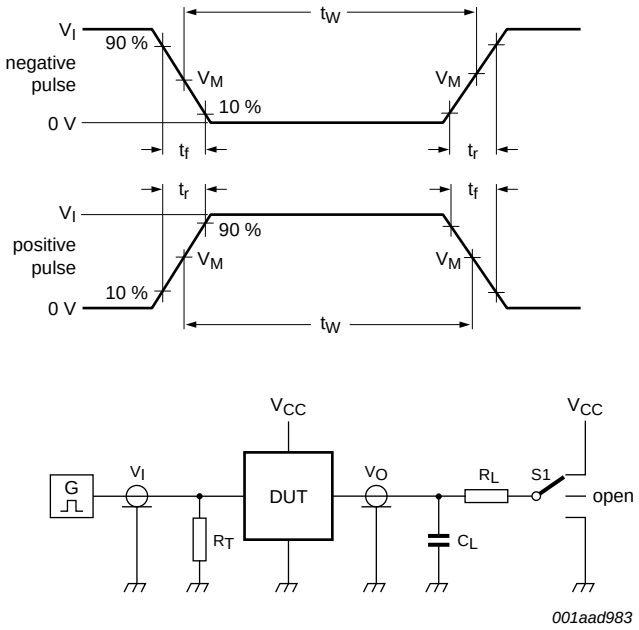

Measurement points are given in Table 9.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 9. Measurement points**

| Type | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 74AHC2G125 | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |
| 74AHCT2G125 | 1.5 V | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 10.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

S1 = Test selection switch.

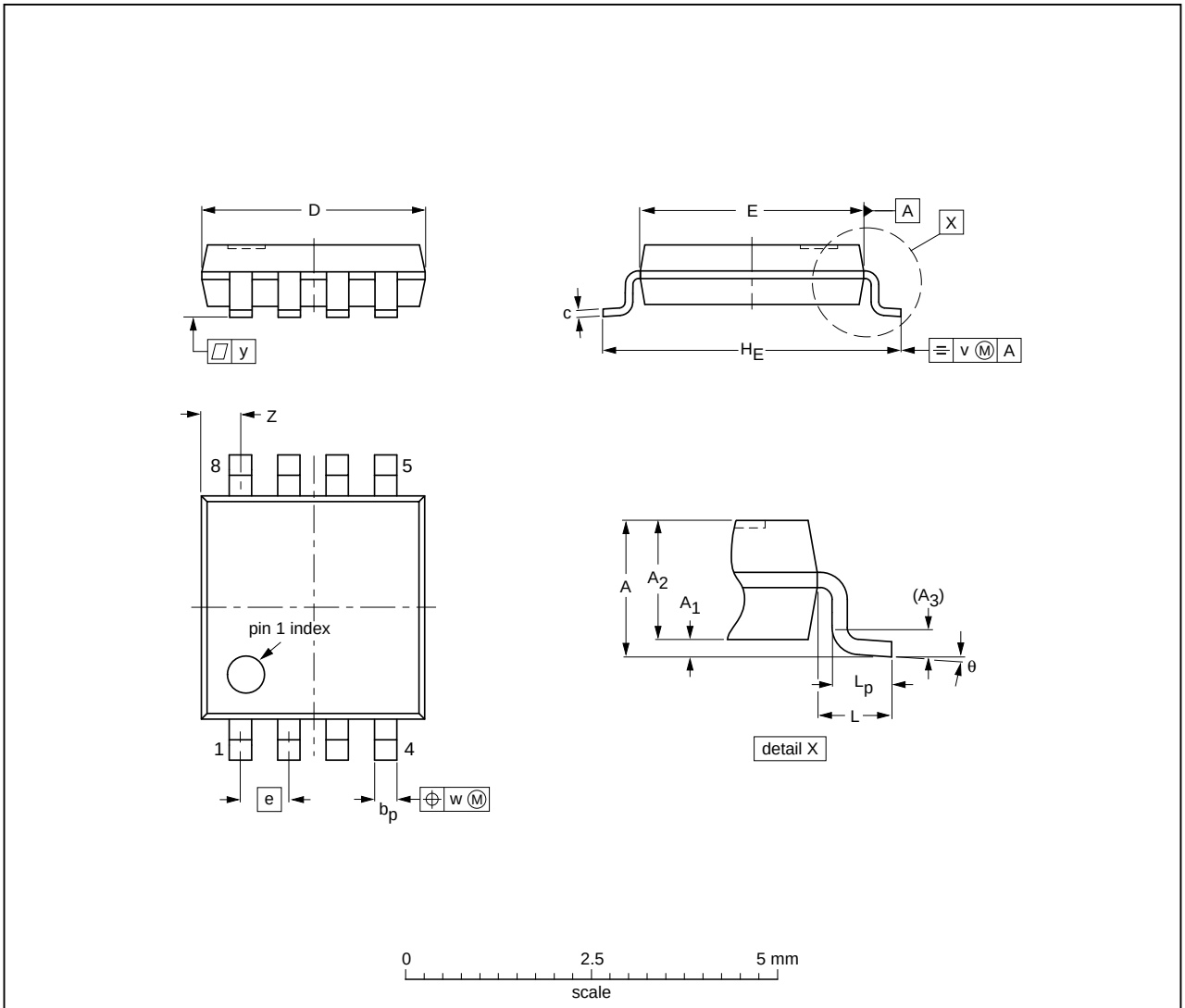
**Fig 8. Test circuit for measuring switching times**

**Table 10. Test data**

| Type | Input | | Load | | S1 position | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 74AHC2G125 | $V_{CC}$ | ≤ 3 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |
| 74AHCT2G125 | 3 V | ≤ 3 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |

## 13. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.00 | 0.95<br>0.75 | 0.25 | 0.38<br>0.22 | 0.18<br>0.08 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 4.1<br>3.9 | 0.5 | 0.47<br>0.33 | 0.2 | 0.13 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

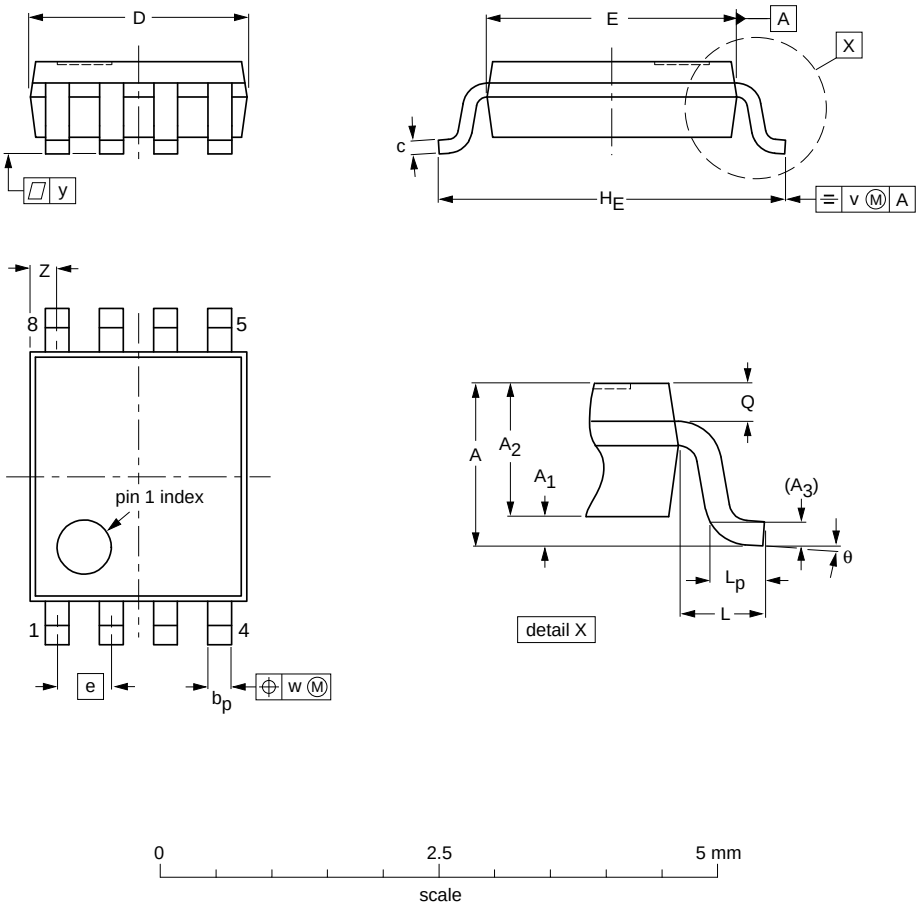
**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | - - - | | | | 02-01-16 |

**Fig 9. Package outline SOT505-2 (TSSOP8)**

**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.15<br>0.00 | 0.85<br>0.60 | 0.12 | 0.27<br>0.17 | 0.23<br>0.08 | 2.1<br>1.9 | 2.4<br>2.2 | 0.5 | 3.2<br>3.0 | 0.4 | 0.40<br>0.15 | 0.21<br>0.19 | 0.2 | 0.13 | 0.1 | 0.4<br>0.1 | 8°<br>0° |

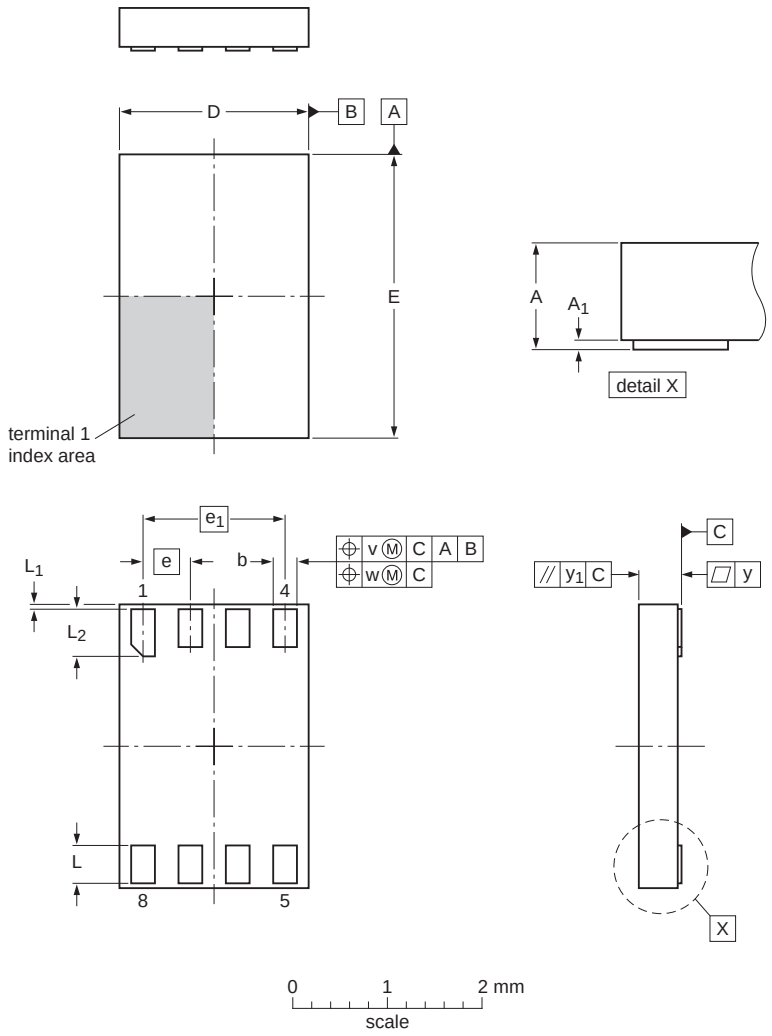
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | 02-06-07 |

**Fig 10. Package outline SOT765-1 (VSSOP8)**

**XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm** **SOT996-2**




Dimensions (mm are the original dimensions)

| Unit[1] | | A | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ | $L_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.5 | 0.05 | 0.35 | 2.1 | 3.1 | 0.5 | 1.5 | 0.5 | 0.15 | 0.6 | 0.1 | 0.05 | 0.05 | 0.1 |
| | nom | | | | | | | | | | | | | | |
| | min | | 0.00 | 0.15 | 1.9 | 2.9 | | | 0.3 | 0.05 | 0.4 | | | | |

*sot996-2_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT996-2 | | | | | | ~~07-12-21~~ 12-11-20 |

**Fig 11. Package outline SOT996-2 (XSON8)**

## 14. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AHC_AHCT2G125 v.3 | 20130506 | Product data sheet | - | 74AHC_AHCT2G125 v.2 |
| Modifications: | • For type number 74AHC2G125GD and 74AHCT2G125GD XSON8U has changed to XSON8. | | | |
| 74AHC_AHCT2G125 v.2 | 20081222 | Product data sheet | - | 74AHC_AHCT2G125 v.1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Added type number 74AHC2G125GD and 74AHCT2G125GD (XSON8U package). | | | |
| 74AHC_AHCT2G125 v.1 | 20040113 | Product specification | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 16.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 16.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations —** A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 18. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 6 May 2013

Document identifier: 74AHC_AHCT2G125